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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,491	02/22/2002	Rajendra Pendse	CPAC 1008-2 US	1495

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EXAMINER
ROMAN, ANGEL

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,491	PENDSE ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 February 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 and 7
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1, 2, 4, 5, 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Jimarez et al. U.S. Patent Application Publication 20010018230.

Jimarez et al. discloses a flip chip package, comprising an integrated circuit chip 12 having interconnect bumps 14 formed on input/output pads in a specified arrangement (see figure 1), and a package substrate 42 having a plurality of bond pads 44 in a complementary arrangement (see figure 5), wherein interconnection between the bumps 14 on the integrated circuit chip 12 and the respective bond pads 44 on the package substrate 42 is established by direct mating of the bump surfaces with the respective bond pads and thermo-mechanical deformation of the bumps (see figure 8). The bump 14 is constructed of a material (lead/tin) selected to provide low yield

strength, high ductility, and an oxidation and corrosion-resistant bump surface. The bumps are formed on the input/output pads of the integrated circuit chip by a solder bumping process (see page 3, paragraph 0058). The bumps may be formed on the input/output pads of the integrated circuit chip by a stud bumping process (see figures 9-16).

Jimarez et al. also discloses a method for forming a flip chip package, comprising providing an integrated circuit chip 12 having interconnect bumps 14 formed on input/output pads in a specified arrangement (see figure 1), each said interconnect bump having low yield strength, high ductility, and an oxidation- and corrosion-resistant surface (formed of a lead/tin composite material); providing a package substrate 42 having a plurality of bond pads 44 in an arrangement complementary to the specified arrangement of input/output pads on the integrated circuit chip (see figure 5); contacting the bumps 14 with the respective bond pads 44 on the package substrate (see figure 7); and thermo-mechanically treating the bumps 14 to form solid-state connections of the bumps with their respective bond pads (see figure 8). The thermo-mechanically treating step comprises concurrently forcing the bump against the pad (force exerted by gravity or pressure by the substrate 12 mounted on substrate 42) and heating the bump and pad (bump reflowing step).

5. Claims 1, 2, 5, 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Pu et al. U.S. Patent 6,350,669 B1.

Pu et al. discloses a flip chip package, comprising an integrated circuit chip 200 having interconnect bumps 222 formed on input/output pads in a specified arrangement, and a package substrate 210 having a plurality of bond pads 211 in a complementary arrangement, wherein interconnection between the bumps 222 on the integrated circuit chip 200 and the respective bond pads 211 on the package substrate 210 is established by direct mating of the bump surfaces with the respective bond pads and thermo mechanical deformation of the bumps (see figures 2A-2C). The bump 222 is constructed of a material (Cu) selected to provide low yield strength, high ductility, and an oxidation- and corrosion-resistant bump surface. The bumps are formed on the input/output pads of the integrated circuit chip by a solder bumping process (see figure 2A).

Pu et al. also discloses a method for forming a flip chip package, comprising providing an integrated circuit chip 200 having interconnect bumps 222 formed on input/output pads in a specified arrangement, each said interconnect bump 222 having low yield strength, high ductility, and an oxidation- and corrosion-resistant surface; providing a package substrate 210 having a plurality of bond pads 211 in an arrangement complementary to the specified arrangement of input/output pads on the integrated circuit chip 200; contacting the bumps 222 with the respective bond pads 211 on the package substrate 210; and thermo-mechanically treating the bumps 222 to form solid-state connections of the bumps 222 with their respective bond pads 211 (see figure 2A-2C). The thermo-mechanically treating step comprises concurrently forcing the bump 222 against the pad 211 and heating the bump and pad (see figure 2C).

6. Claims 1, 5, 9-11, 13-16, 18 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Jimarez et al. U.S. Patent 6,191,952 B1.

Jimarez et al. discloses a flip chip package, comprising an integrated circuit chip 12 having interconnect bumps 16 formed on input/output pads in a specified arrangement, and a package substrate 22 having a plurality of bond pads 24 in a complementary arrangement, wherein interconnection between the bumps on the integrated circuit chip and the respective bond pads on the package substrate is established by direct mating of the bump surfaces with the respective bond pads and thermo-mechanical deformation of the bumps (see figure 3). The flip chip package, also comprises an integrated circuit chip 12 having interconnect bumps 16 formed on input/output pads in a specified arrangement in a surface thereof, and a package substrate 22 having a plurality of bond pads 24 in a complementary arrangement in a subjacent surface of the package substrate, wherein second level interconnect sites are arranged in a second surface of the package substrate, and second level interconnect structures are connected to the respective second level interconnect sites, and wherein a fill volume is defined between the integrated circuit chip 12 and the package substrate 22 (see figure 3), the fill volume being at least partly filled with at least one fill material, each said fill material having a selected specific elastic modulus, wherein regions 68 of the fill volume that overlie the second level interconnect sites contain a lower specific elastic modulus fill material (see Abstract). The fill volume includes a first fill zone 68 comprising a plurality of generally columnar volumes, generally overlying the plurality of

second level interconnect sites; and the second fill zone 48 consists of the remainder of the fill volume (see figure 3). At least a part of the first fill zone contains a first material having a lower specific elastic modulus, and at least a part of the second fill zone contains a second material having a higher specific elastic modulus (see Abstract). The second fill material has a specific elastic modulus greater than about 5 GPa or in a range of about 5 GPa to about 15 GPa (see column 1, lines 50-53). The second fill material may comprise a silicon adhesive or an anhydride curable epoxy (see column 4, lines 18-26). The bumps are formed on the input/output pads of the integrated circuit chip by a solder bumping process. The thermo-mechanically treating step comprises concurrently forcing the bump against the pad and heating the bump and pad (see column 2, lines 60-63).

Jimarez et al. also discloses a method for making a flip chip package configured for interconnection to a printed circuit board 32, comprising providing an integrated circuit chip 12 having a surface; providing a package substrate 22 having a first surface and a second surface, the second surface being provided with a plurality of second level interconnect sites, the locations of the second level interconnect sites defining a plurality of first fill zone areas over the first surface of the package substrate, the remainder of the first surface of the package substrate constituting a second fill zone area; dispensing at least a second fill material 48, having a specific elastic modulus greater than about 5 GPa, within the second fill zone area on the first surface of the package substrate 22; and assembling the integrated circuit chip 12 and the package substrate 22 so that the second fill material 48 is confined in a second fill zone within a volume

defined between the integrated circuit chip 12 surface and the first surface of the package substrate 22 (see figure 3).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jimarez et al. U.S. Patent Application Publication 20010018230.

Jimarez et al. is applied as above but lacks anticipation on forming the bumps of gold or a gold alloy material; and forming the bumps on the input/output pads of the integrated circuit chip by an electroplating process.

With respect to forming the bumps of gold or a gold alloy material, the particular type of material used to make the bumps, is only considered to be the use of a " preferred " or " optimum " material out of a plurality of well known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation based, among other things, on a desire costs and product reliability.

Regarding forming the bumps on the input/output pads of the integrated circuit chip by an electroplating process, forming metal bumps by using electroplating processes is well known in the art of manufacturing metal bumps and a person having ordinary skills in the art at the time the invention was made would have been able to use a metal electroplating process to form the metal bumps in the primary reference of Jimarez et al. based on a desire process manufacturing cost and accuracy. Furthermore using a metal electroplating process in the primary reference of Jimarez et al. is only considered to be routine optimization of the processes and devices disclosed by Jimarez et al. since Jimarez et al. is already forming metal bumps, therefore selecting an "optimum" bump forming process for forming the metal bumps in the primary reference of Jimarez et al. could be performed by routine experimentation.

10. Claims 2-4, 6-8, 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jimarez et al. U.S. Patent 6,191,952 B1.

Jimarez et al. is applied as above but lacks anticipation on disclosing an optimum preferred material selected to provide low yield strength, high ductility, and an oxidation-

and corrosion-resistant bump surface, e.g. gold, for forming the solder bumps; disclosing different process of forming the solder bumps, e.g. electroplating or stud bumping; and disclosing a specific elastic modulus of less than about 0.5 Gpa for the first fill material.

With respect to disclosing an optimum preferred material selected to provide low yield strength, high ductility, and an oxidation- and corrosion-resistant bump surface, e.g. gold, for forming the solder bumps the particular type of material used to make the bumps, is only considered to be the use of a " preferred " or " optimum " material out of a plurality of well known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation based, among other things, on a desire costs and product reliability.

Regarding forming the bumps on the input/output pads of the integrated circuit chip by an electroplating or stud bumping process, forming metal bumps by using electroplating or stud bumping processes is well known in the art of manufacturing metal bumps and a person having ordinary skills in the art at the time the invention was made would have been able to use metal electroplating or stud bumping processes to form the metal bumps in the primary reference of Jimarez et al. based on a desire process manufacturing cost and accuracy. Furthermore using a metal electroplating or stud bumping processes in the primary reference of Jimarez et al. is only considered to be routine optimization of the processes and devices disclosed by Jimarez et al. since Jimarez et al. is already forming metal bumps, therefore selecting an "optimum" bump

forming process for forming the metal bumps in the primary reference of Jimarez et al. could be performed by routine experimentation.

As to disclosing a specific elastic modulus of less than about 0.5 GPa for the first fill material, Jimarez et al. discloses an underfill material 48 having a modulus greater than 2 GPa and a first fill material 68 with a modulus less than about one half the modulus of the underfill 48 (see column 4, lines 6-18), therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a specific elastic modulus of less than about 0.5 GPa for the first fill material in the primary reference of Jimarez et al. since 0.5 GPa is less than one half of 2 GPa. Furthermore selecting an optimum modulus value of less than about 0.5 GPa may be obtain by performing routine experimentation and selecting the optimum material of the materials already suggested by Jimarez et al.

11. Claims 9-11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al. U.S. Patent 5,956,605 A in view of Jimarez et al. U.S. Patent 6,191,952 B1.

Akram et al. discloses a flip chip package, comprising an integrated circuit chip 12 having interconnect bumps 16 formed on input/output pads 14 in a specified arrangement in a surface thereof, and a package substrate 42 having a plurality of bond pads 44 in a complementary arrangement in a subjacent surface of the package substrate 42, wherein a fill volume is defined between the integrated circuit chip and the package substrate, the fill volume being at least partly filled with at least one fill material,

each said fill material having a selected specific elastic modulus. The fill volume includes a first fill zone comprising a plurality of generally columnar volumes; and a second fill zone consisting of the remainder of the fill volume (see figure 4). At least a part of the first fill zone contains a first material (void space) having a lower specific elastic modulus, and at least a part of the second fill zone contains a second material (silicon nitride) having a higher specific elastic modulus.

Akram et al. is applied as above but lacks anticipation on disclosing interconnection sites arranged in a second surface of the package substrate 42 underlying the void spaces and second level interconnect structures connected to the respective second level interconnect sites, Jimarez et al. discloses interconnection sites arranged in a second surface of a package substrate having second level interconnect structures connected to the respective second level interconnect sites (see figure 3) in view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose second interconnection sites arranged in a second surface of the package substrate 42 underlying the void spaces and second level interconnect structures connected to the respective second level interconnect sites, as disclose in Jimarez et al. in the primary reference of Akram et al. since Akram et al. suggest pads 44 being in communication with conductive traces on or within substrate 42 (see column 7, lines 1-10).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Capote et al., Amador et al. and Tanaka discloses flip chip package devices comprising plural underfill materials having different modulus coefficients. Farnworth et al. discloses a flip chip package device comprising gold bumps. Lin et al. discloses a flip chip package device comprising a combined underfill material.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

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October 16, 2002